Docket No : 50006-070 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

iro MATSUFUSA, et al. :

Serial No.: 09/620,718 : Group Art Unit: 2814

Filed: July 20, 2000 : Examiner: G. Peralta

For: SEMICONDUCTOR DEVICE HAVING TEST MARK

THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	8	20	0	$18.00 =	$0.00
Independent Claims	1	3	0	$84.00 =	$0.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$0.00
					$0.00
				Total of Above Calculations	$0.00

☐ Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Date: September 18, 2002

Docket No.: 50006-07

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In re Application of	:	
Jiro MATSUFUSA, et al.	:	
Serial No.: 09/620,718	:	Group Art Unit: 2814
Filed: July 20, 2000	:	Examiner: Ginette PERALTA

For: SEMICONDUCTOR DEVICE HAVING TEST MARK

AMENDMENT UNDER 37 C.F.R. 1.111

Commissioner for Patents
Washington, DC 20231

Sir:

In response to the June 19, 2002 non-final Office Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend/replace claim 1 as follows:

1. (Amended) A semiconductor device having a test mark comprising:

a semiconductor substrate;

a first TEOS layer formed on said semiconductor substrate;

a second TEOS layer formed on said first TEOS layer and having a lower fluidity than that of said first TEOS layer at an elevated temperature;

a recess formed in said first and second TEOS layers and exposing the surface of said semiconductor substrate, wherein the horizontal cross-section of said recess is substantially